STRUCTURE AND METHOD TO FORM SOURCE AND DRAIN REGIONS OVER DOPED DEPLETION REGIONS

ABSTRACT

A structure and method of reducing junction capacitance of a source/drain region in a transistor. A gate structure is formed over on a first conductive type substrate. We perform a doped depletion region implantation by implanting ions being the second conductive type to the substrate using the gate structure as a mask, to form a doped depletion region beneath and separated from the source/drain regions. The doped depletion regions have an impurity concentration and thickness so that the doped depletion regions are depleted due to a built-in potential creatable between the doped depletion regions and the substrate. The doped depletion region and substrate form depletion regions between the source/drain regions and the doped depletion region. We perform a S/D implant by implanting ions having a second conductivity type into the substrate to form S/D regions. The doped depletion region and depletion regions reduce the capacitance between the source/drain regions and the substrate.